

# 8-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-8L MB89810A Series

### MB89816A/P817A

#### ■ DESCRIPTION

The MB89810A series is a line of single-chip microcontrollers based on the F<sup>2</sup>MC\*-8L CPU core which can operate at low voltage but at high speed. The microcontrollers contain peripheral function such as timer, serial interface, a UART, and an external interrupt. The MB89810A series is applicable to a wide range of applications from welfare products to industrial equipment, including portable devices.

\*: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

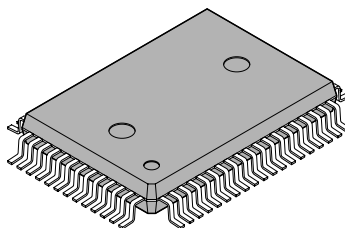
#### ■ FEATURES

- High speed processing at low voltage  
Minimum execution time: 0.8  $\mu$ s/3.0 V, 1.33  $\mu$ s/2.2 V
- F<sup>2</sup>MC-8L family CPU core
  - Instruction set optimized for controllers : Multiplication and division instructions  
16-bit arithmetic operations  
Test and branch instructions  
Bit manipulation instructions, etc.
- Four types of timers
  - 8-bit PWM timer: 2 channels (also serve as reload timers)
  - 16-bit timer/counter
  - 21-bit time-base timer

(Continued)

#### ■ PACKAGE

64-pin Plastic QFP



(FPT-64P-M06)

# MB89810A Series

*(Continued)*

- Two serial interface  
8-bit synchronous serial (Switchable transfer direction allows communication with various equipment.)  
UART (5-, 7-, or 8-bit transfer capable)
- External interrupt: 8 channels  
Eight channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes  
Stop mode (Oscillation stops to minimize the current consumption)  
Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal)

# MB89810A Series

## ■ PRODUCT LINEUP

| Part number<br>Parameter | MB89816A   | MB89P817A   |
|--------------------------|--|---|
| Classification           | Mass-production product<br>(mask ROM products)   | One-time PROM product<br>(for evaluation and development)                           |
| ROM size                 | 24 K × 8 bits<br>(internal mask ROM)   | 32 K × 8 bits<br>(internal PROM, programming with general-purpose EPROM programmer) |
| RAM size                 | 2048 × 8 bits  |   |
| CPU functions            | Number of instructions: 136<br>Instruction bit length: 8 bits<br>Instruction length: 1 to 3 bytes<br>Data bit length: 1, 8, 16 bits<br>Minimum execution time: 0.8 μs/5 MHz<br>Interrupt processing time: 7.2 μs/5 MHz   |   |
| Ports                    | Input ports: 8 (All also serve as peripherals.)<br>Output ports: 8<br>I/O ports (N-ch open-drain): 5 (for LED driving)<br>I/O ports (CMOS): 32 (14 ports also serve as peripherals.)<br>Total: 53  |   |
| 8-bit PWM timer          | Two internal channels<br>8-bit reload timer operation (toggled output capable, operating clock cycle: 3 different cycles)<br>8-bit resolution PWM operation (conversion cycle: 3 different cycles)   |   |
| 8-bit timer/counter      | 16-bit timer operation<br>16-bit event counter operation   |   |
| UART                     | 5-, 7-, or 8-bit transfer capable<br>Built-in baud rate generator<br>Clock synchronous/asynchronous data transfer capable  |   |
| 8-bit Serial I/O         | 8-bits<br>LSB-first/MSB first selectability<br>One clock selectable from four transfer clocks<br>(one external shift clock, three internal shift clocks)   |   |
| External interrupt       | 8 independent channels (edge selection, interrupt vector, source flag)<br>4 channels: Level detection (level selectable)<br>4 channels: Edge detection (edge selectable)<br>Used also for wake-up from the stop/sleep mode. (Edge detection is also permitted in stop mode.) |   |

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# MB89810A Series

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| Part number<br>Parameter | MB89816A  | MB89P817A       |
|--------------------------|---|-----------------|
| Watch interrupt          | Interrupt cycles: 4 different cycles (subclock) |                 |
| Watchdog timer reset     | Reset occurrence cycle: 839 ms/5 MHz            |                 |
| Standby mode             | Sleep mode, stop mode                           |                 |
| Process                  | CMOS  |                 |
| Package                  | FPT-64P-M06                                     |                 |
| Operating voltage        | 2.2 V to 6.0 V*                                 | 2.7 V to 6.0 V* |

\*: Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products, verify its differences from the product that will actually be used.

### 2. Current Consumption

When operated at low speed, the product with an OTPROM will consume more current than the product with a mask ROM.

However, the same is current consumption in sleep/stop modes (For more information, see “■ ELECTRICAL CHARACTERISTICS”).

### 3. Mask Options

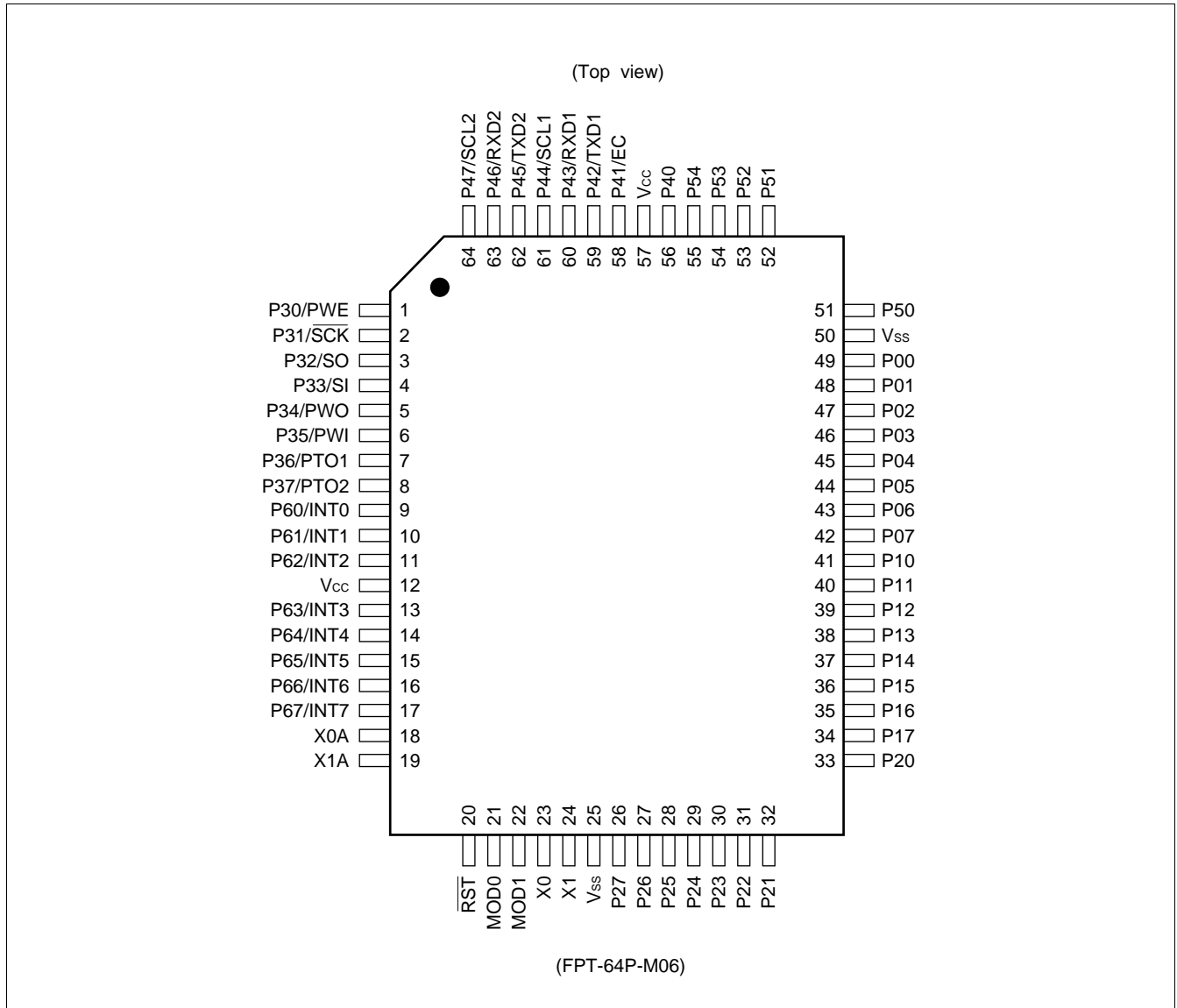
Functions that can be selected as options and how to designate these options vary with product.

Before using options, check “■ MASK OPTIONS”.

Take particular care on the following point:

For MB89816A, pull-up resistor option can be set for P50 to P54.

## PIN ASSIGNMENT



# MB89810A Series

## ■ PIN DESCRIPTION

| Pin no.  | Pin name                     | Circuit type | Function  |
|----------|------------------------------|--------------|---|
| 23       | X0                           | A            | Main clock oscillator pins  |
| 24       | X1                           |              |   |
| 18       | X0A                          | I            | Subclock crystal oscillator pins  |
| 19       | X1A                          |              |   |
| 21       | MOD0                         | B            | Operating mode selection pins<br>Connect directly these pins directly to V <sub>SS</sub> .  |
| 22       | MOD1                         |              |   |
| 20       | $\overline{\text{RST}}$      | C            | Reset I/O pin<br>This pin is an N-ch open-drain output type with a pull-up resistor and a hysteresis input type.<br>“L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”. |
| 49 to 42 | P00 to P07                   | D            | General-purpose I/O ports<br>A pull-up resistor option is provided.<br>These ports have the port output inverting function.   |
| 41 to 34 | P10 to P17                   | D            | General-purpose I/O ports<br>A pull-up resistor option is provided.<br>These ports have the port output inverting function.   |
| 33 to 30 | P20 to P23                   | F            | General-purpose output ports<br>These ports have the port output inverting function.  |
| 29 to 26 | P24 to P27                   | F            | General-purpose output ports  |
| 1        | P30 /PWE                     | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as a pulse width detection enable input (PWE).<br>PWE input is hysteresis input.  |
| 2        | P31/ $\overline{\text{SCK}}$ | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the clock I/O for the 8-bit serial I/O (SCK).<br>SCK input is hysteresis input.  |
| 3        | P32/SO                       | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data output for the 8-bit serial I/O (SO).   |
| 4        | P33/SI                       | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data input for the 8-bit serial I/O (SI).<br>SI input is hysteresis input.   |
| 5        | P34/PWO                      | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as a pulse width detection output (PWO).  |
| 6        | P35/PWI                      | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as a pulse width detection input (PWI).<br>PWI input is hysteresis input.   |
| 7        | P36/PTO1                     | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the toggle output for the 8-bit PWM timer 1 (PTO1).  |

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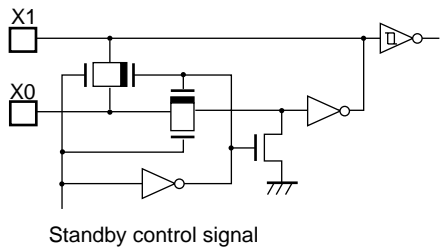
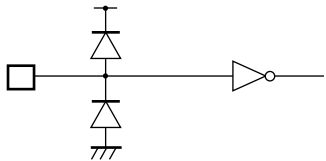
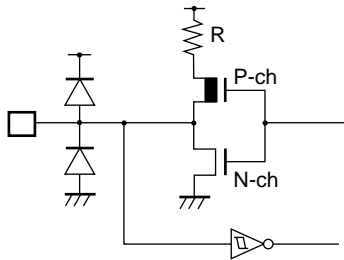
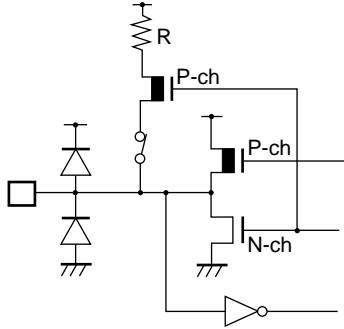
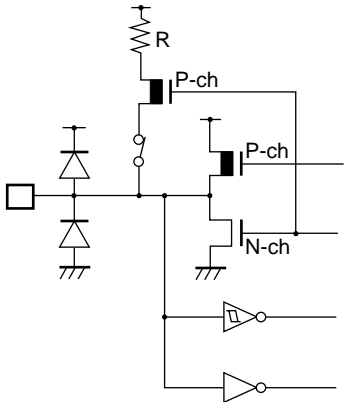
# MB89810A Series

(Continued)

| Pin no.  | Pin name                | Circuit type | Function   |
|----------|-------------------------|--------------|--|
| 8        | P37/PTO2                | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the toggle output for the 8-bit PWM timer 2 (PTO2).                                     |
| 56       | P40                     | D            | General-purpose I/O port<br>A pull-up resistor option is provided.   |
| 58       | P41/EC                  | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as a 16-bit timer/counter input (EC).<br>EC input is hysteresis input.                     |
| 59       | P42/TXD1                | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data output 1 for the UART (TXD1).  |
| 60       | P43/RXD1                | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data input 1 for the UART (RXD1).<br>RXD1 input is hysteresis input.                |
| 61       | P44/SCL1                | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the clock I/O 1 for the UART (SCL1).<br>SCL1 input is hysteresis input.                 |
| 62       | P45/TXD2                | D            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data output 2 for the UART (TXD2).  |
| 63       | P46/RXD2                | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the data input 2 for the UART (RXD2).<br>RXD2 input is hysteresis input.                |
| 64       | P47/SCL2                | E            | General-purpose I/O port<br>A pull-up resistor option is provided.<br>Also serves as the clock I/O 2 for the UART (SCL2).<br>SCL2 input is hysteresis input.                 |
| 51 to 55 | P50 to P54              | G            | N-channel open-drain I/O ports<br>A pull-up resistor option is provided only for the MB89816A.   |
| 9 to 11  | P60/INT0 to<br>P62/INT2 | H            | General-purpose I/O ports<br>A pull-up resistor option is provided.<br>Also serve as an external interrupt input (INT0 to INT2).<br>These ports are a hysteresis input type. |
| 13 to 17 | P63/INT3 to<br>P67/INT7 | H            | General-purpose I/O ports<br>A pull-up resistor option is provided.<br>Also serve as an external interrupt input (INT3 to INT7).<br>These ports are a hysteresis input type. |
| 12, 57   | V <sub>cc</sub>         | –            | Power supply pin   |
| 25, 50   | V <sub>ss</sub>         | –            | Power supply (GND) pin   |

# MB89810A Series

## I/O CIRCUIT TYPE

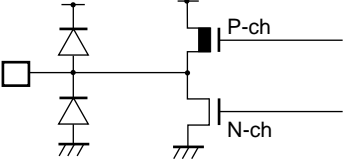
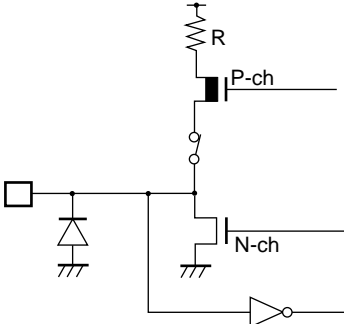
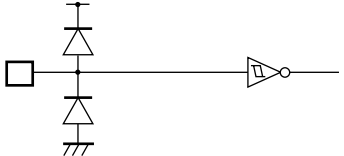
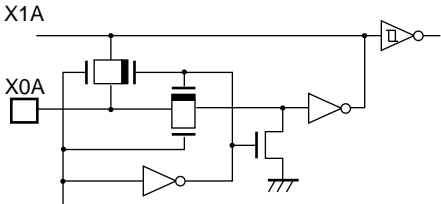
| Type | Circuit   | Remarks   |
|------|---|---|
| A    |  <p>Standby control signal</p> | <ul style="list-style-type: none"> <li>• Main clock</li> <li>• At an oscillation feedback resistor of approximately 1 MΩ (1 to 5 MHz)</li> <li>• CR oscillator circuit selectability</li> </ul> |
| B    |                                |   |
| C    |                               | <ul style="list-style-type: none"> <li>• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V</li> <li>• Hysteresis input</li> </ul>   |
| D    |                              | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> </ul> <p>• Pull-up resistor optional</p>  |
| E    |                              | <ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input (resource input)</li> </ul> <p>• Pull-up resistor optional</p>                           |

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# MB89810A Series

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| Type | Circuit   | Remarks   |
|------|---|---|
| F    |    | <ul style="list-style-type: none"> <li>• CMOS output</li> </ul>   |
| G    |    | <ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• CMOS input</li> <li>• Pull-up resistor optional (only for the MB89816A)</li> </ul> |
| H    |   | <ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-up resistor optional</li> </ul>   |
| I    |  | <ul style="list-style-type: none"> <li>• Subclock (30 to 40 kHz)</li> <li>• At an oscillation feedback resistor of approximately 10 MΩ</li> </ul>             |

# MB89810A Series

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Power Supply Voltage Fluctuations

Although  $V_{CC}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 4. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

## PROGRAMMING TO THE EPROM ON THE MB89P817A

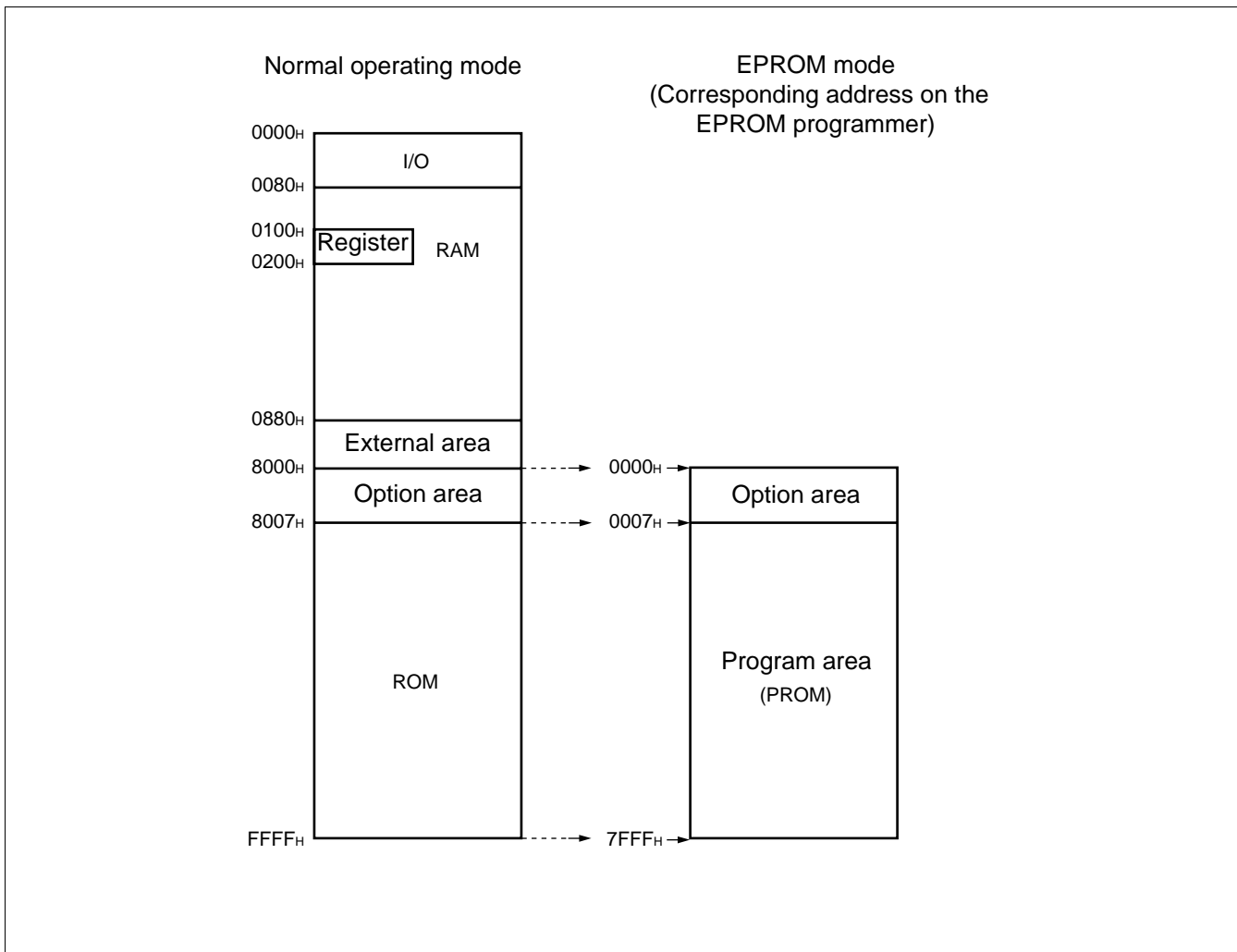
In EPROM mode, the MB89P817A functions equivalent to the MBM27C256A. This allows the OTPROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

### • Writing Procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0007<sub>H</sub> to 7FFF<sub>H</sub> (note that addresses 8007<sub>H</sub> to FFFF<sub>H</sub> while operating as operating mode assign to 0007<sub>H</sub> to 7FFF<sub>H</sub> in EPROM mode).  
Load option data into addresses 0000<sub>H</sub> to 0006<sub>H</sub> of the EPROM programmer. (For information about each corresponding option, see “• OTPROM Option Bit Map.”)
- (3) Program with the EPROM programmer.

### • Memory Space

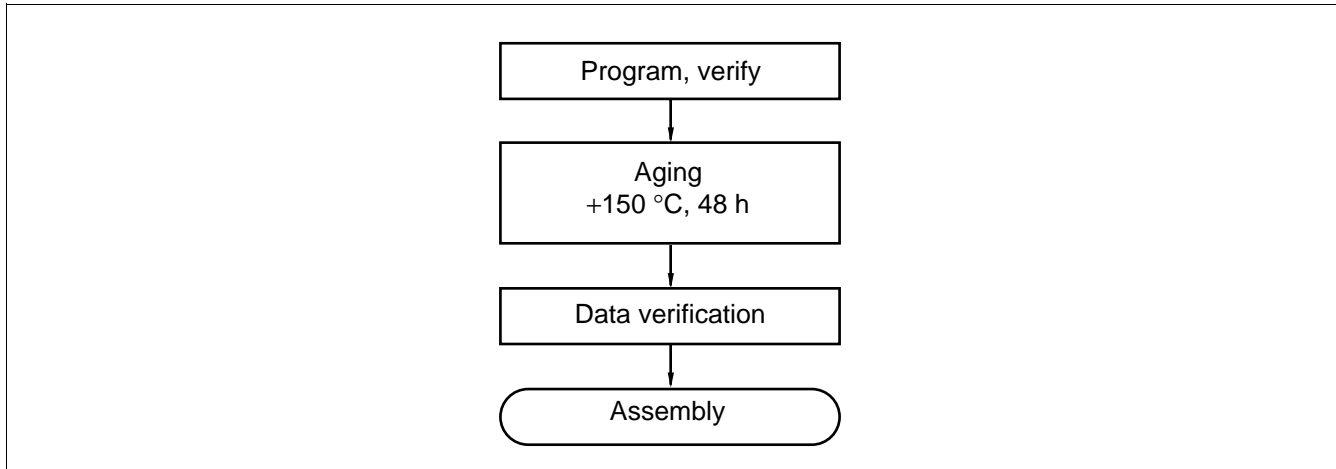
Memory space is diagrammed below.



# MB89810A Series

- **Recommended Screening Conditions**

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM (one-time PROM) microcomputer program.



- **Programming Yield**

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

- **EPROM Programmer Socket Adapter**

| Package     | Compatible socket adapter |
|-------------|---------------------------|
| FPT-64P-M06 | ROM-64QF-28DP-8L          |

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Connect the jumper pin to  $V_{SS}$  when using.

Depending on the EPROM programmer, inserting a capacitor of approx. 0.1  $\mu$ F between  $V_{PP}$  and  $V_{SS}$  or  $V_{CC}$  and  $V_{SS}$  can stabilize programming operations.

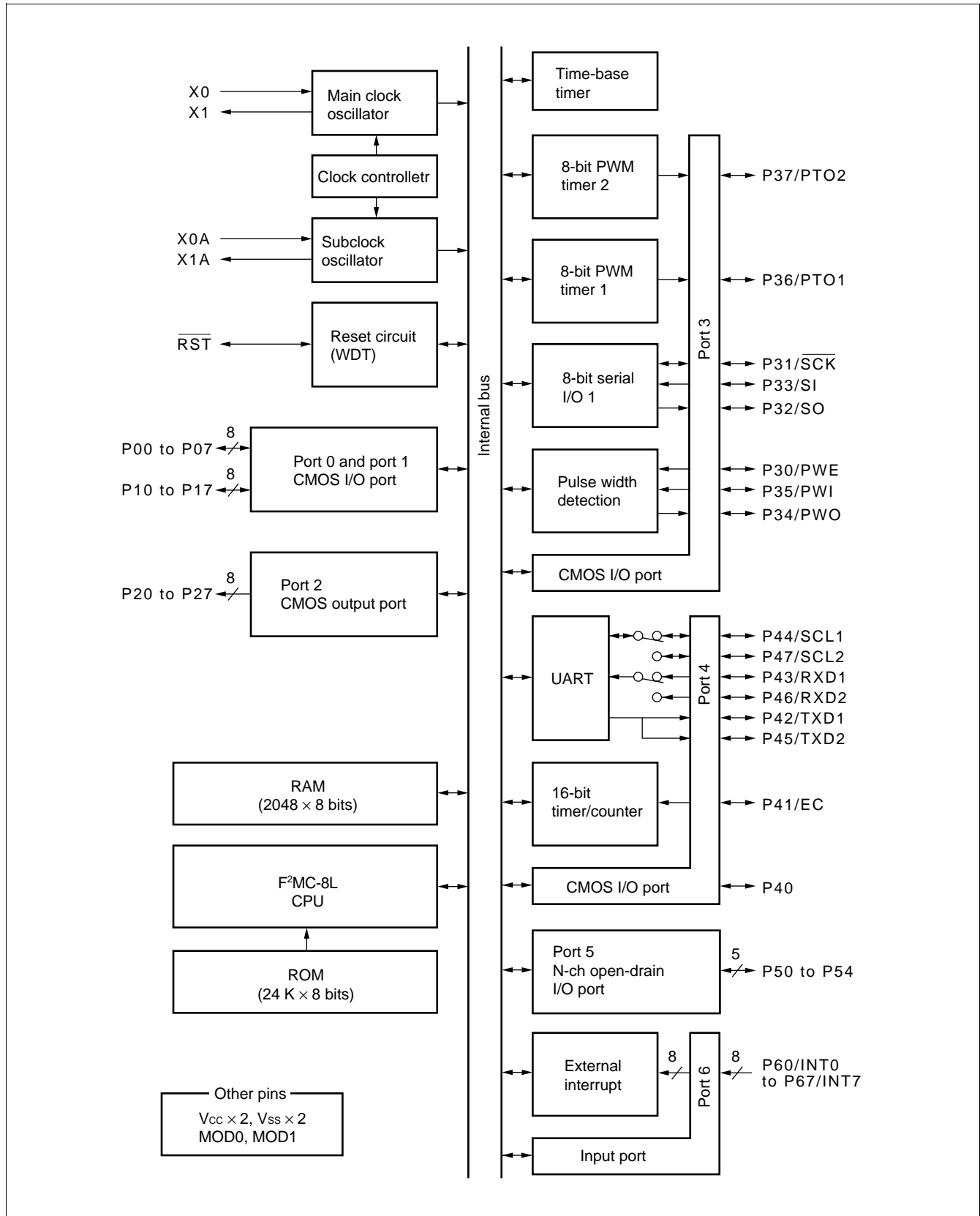
• **OTPROM Option Bit Map**

|                       | Bit 7                                | Bit 6                                | Bit 5                                | Bit 4                                | Bit 3                                      | Bit 2                          | Bit 1   | Bit 0  |
|-----------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--|--------------------------------|---|--|
| 000<br>0 <sub>H</sub> | Vacancy                              | Vacancy                              | Vacancy                              | Single-clock setting                 | Reset pin output                           | Power-on reset                 | Oscillation stabilization time  |  |
|                       | Readable and writable                | Readable and writable                | Readable and writable                | 1: Dual-clock<br>0: Single-clock     | 1: Enabled<br>0: Disabled                  | 1: Enabled<br>0: Disabled      | 00 2 <sup>4</sup> /F <sub>CH</sub><br>10 2 <sup>17</sup> /F <sub>CH</sub> | 01 2 <sup>14</sup> /F <sub>CH</sub><br>11 2 <sup>18</sup> /F <sub>CH</sub> |
| 000<br>1 <sub>H</sub> | P07 Pull-up<br>1: No<br>0: Yes       | P06 Pull-up<br>1: No<br>0: Yes       | P05 Pull-up<br>1: No<br>0: Yes       | P04 Pull-up<br>1: No<br>0: Yes       | P03 Pull-up<br>1: No<br>0: Yes             | P02 Pull-up<br>1: No<br>0: Yes | P01 Pull-up<br>1: No<br>0: Yes  | P00 Pull-up<br>1: No<br>0: Yes   |
| 000<br>2 <sub>H</sub> | P17 Pull-up<br>1: No<br>0: Yes       | P16 Pull-up<br>1: No<br>0: Yes       | P15 Pull-up<br>1: No<br>0: Yes       | P14 Pull-up<br>1: No<br>0: Yes       | P13 Pull-up<br>1: No<br>0: Yes             | P12 Pull-up<br>1: No<br>0: Yes | P11 Pull-up<br>1: No<br>0: Yes  | P10 Pull-up<br>1: No<br>0: Yes   |
| 000<br>3 <sub>H</sub> | P37 Pull-up<br>1: No<br>0: Yes       | P36 Pull-up<br>1: No<br>0: Yes       | P35 Pull-up<br>1: No<br>0: Yes       | P34 Pull-up<br>1: No<br>0: Yes       | P33 Pull-up<br>1: No<br>0: Yes             | P32 Pull-up<br>1: No<br>0: Yes | P31 Pull-up<br>1: No<br>0: Yes  | P30 Pull-up<br>1: No<br>0: Yes   |
| 000<br>4 <sub>H</sub> | P47 Pull-up<br>1: No<br>0: Yes       | P46 Pull-up<br>1: No<br>0: Yes       | P45 Pull-up<br>1: No<br>0: Yes       | P44 Pull-up<br>1: No<br>0: Yes       | P43 Pull-up<br>1: No<br>0: Yes             | P42 Pull-up<br>1: No<br>0: Yes | P41 Pull-up<br>1: No<br>0: Yes  | P40 Pull-up<br>1: No<br>0: Yes   |
| 000<br>5 <sub>H</sub> | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | P64 Pull-up<br>1: No<br>0: Yes       | P63 Pull-up<br>1: No<br>0: Yes             | P62 Pull-up<br>1: No<br>0: Yes | P61 Pull-up<br>1: No<br>0: Yes  | P60 Pull-up<br>1: No<br>0: Yes   |
| 000<br>6 <sub>H</sub> | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Vacancy<br><br>Readable and writable | Oscillator type<br><br>1: Crystal<br>0: CR | P67 Pull-up<br>1: No<br>0: Yes | P66 Pull-up<br>1: No<br>0: Yes  | P65 Pull-up<br>1: No<br>0: Yes   |

Note: • Each bit is set to '1' as the initialized value.  
 • Do not write '0' to the vacant bit.

# MB89810A Series

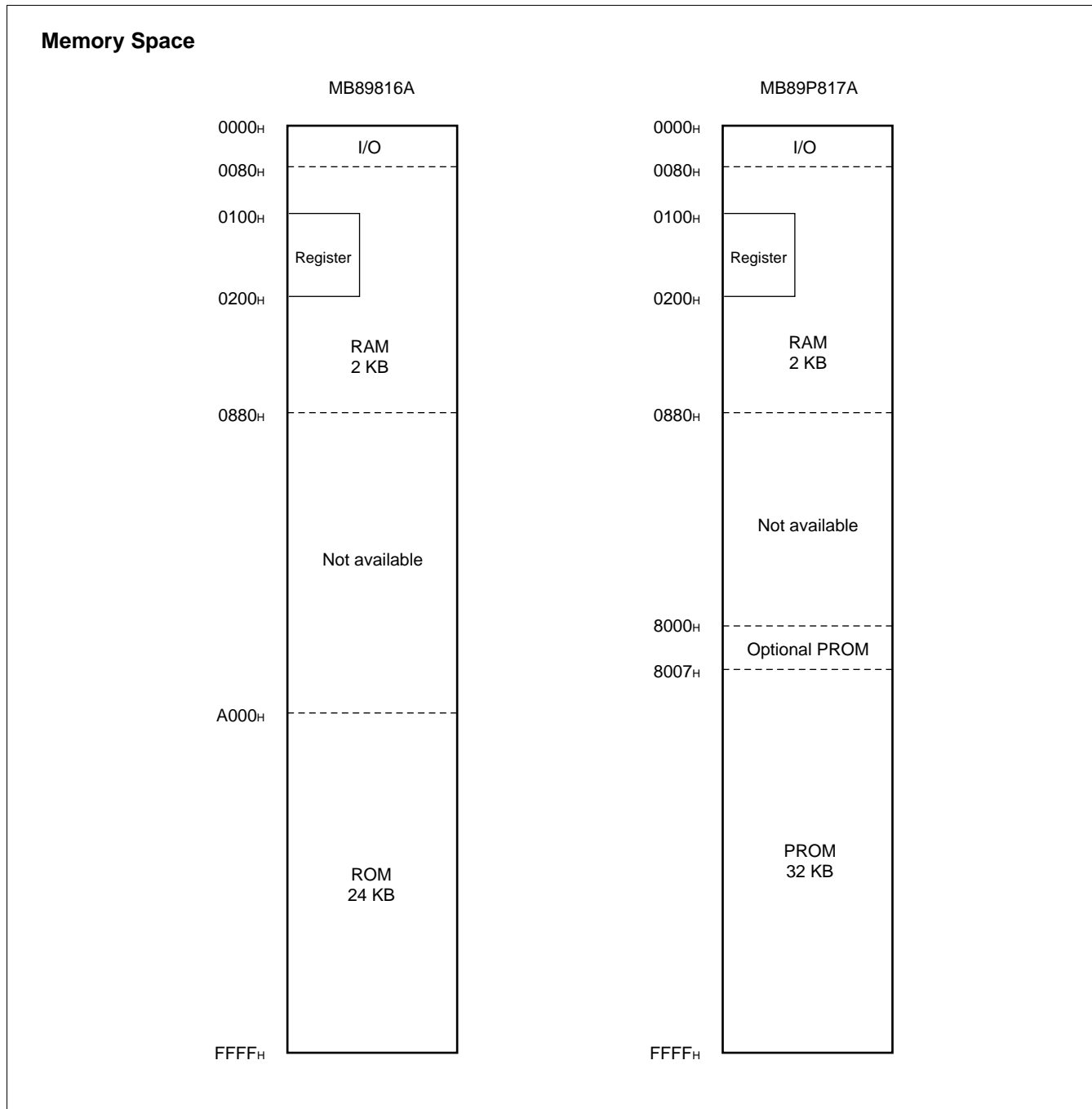
## ■ BLOCK DIAGRAM



## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89810A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89810A series is structured as illustrated below.

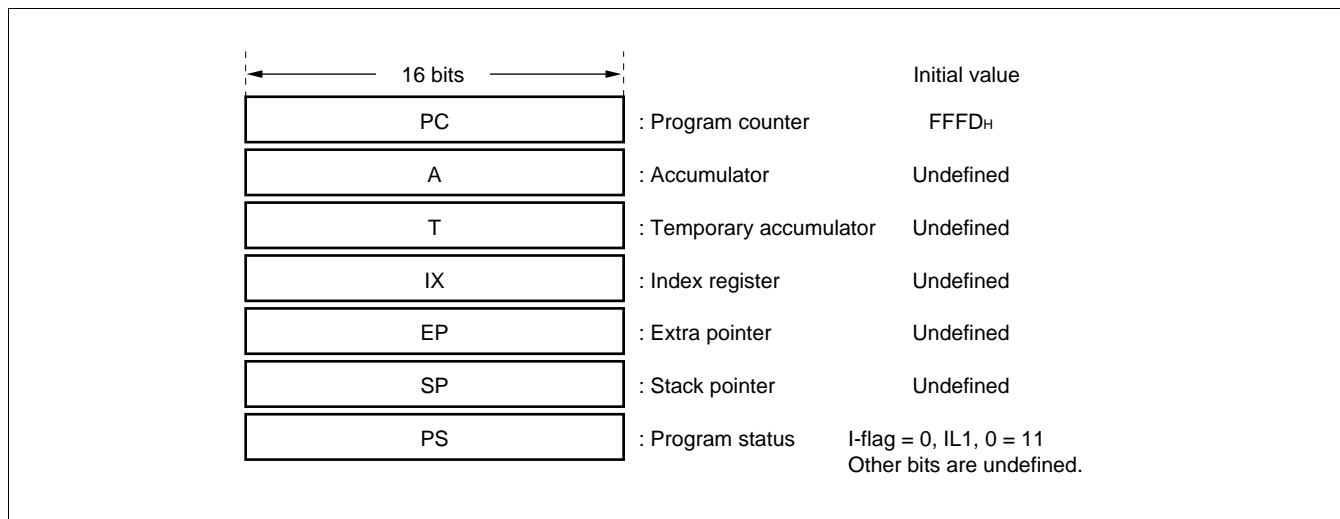


# MB89810A Series

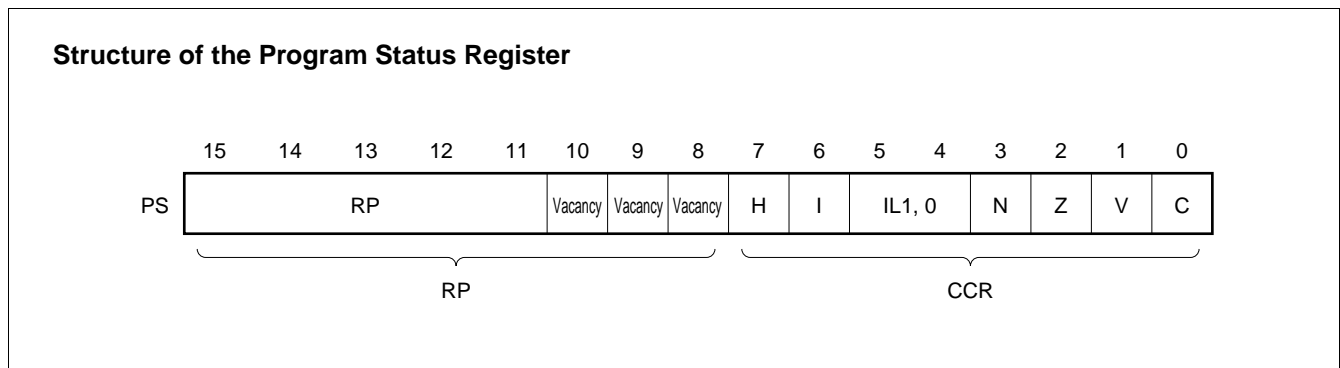
## 2. Registers

The F<sup>2</sup>MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification
- Extra pointer (EP): A 16-bit pointer for indicating a memory address
- Stack pointer (SP): A 16-bit register for indicating a stack area
- Program status (PS): A 16-bit register for storing a register pointer, a condition code



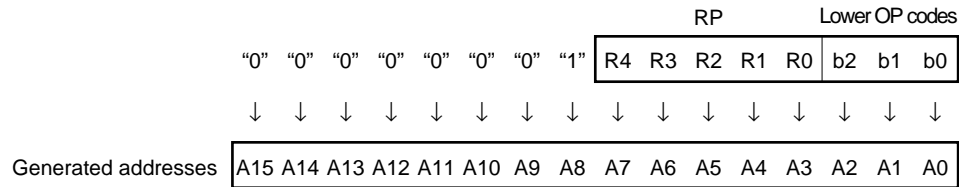
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)





The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

### Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

**H-flag:** Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

**I-flag:** Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

**IL1, 0:** Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | ILO | Interrupt level | High-low                             |
|-----|-----|-----------------|--------------------------------------|
| 0   | 0   | 1               | High<br>↑<br>↓<br>Low = no interrupt |
| 0   | 1   |                 |                                      |
| 1   | 0   | 2               |                                      |
| 1   | 1   | 3               |                                      |

**N-flag:** Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

**Z-flag:** Set when an arithmetic operation results in 0. Cleared otherwise.

**V-flag:** Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

**C-flag:** Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

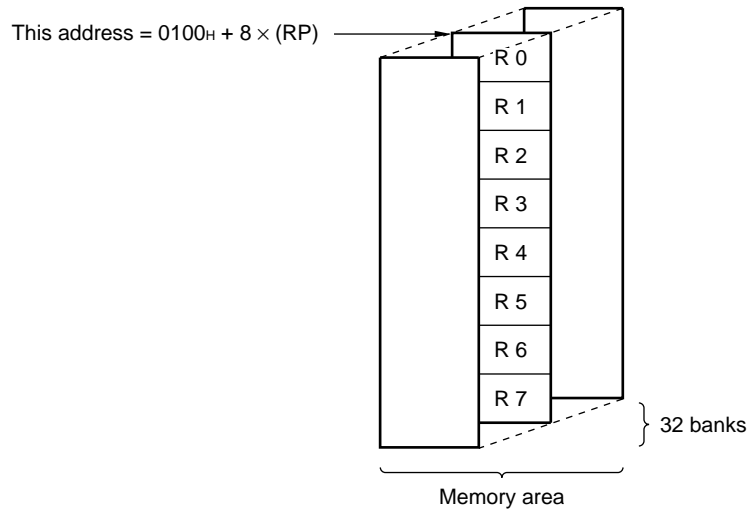
# MB89810A Series

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89816A. The bank currently in use is indicated by the register bank pointer (RP).

## Register Bank Configuration



## ■ I/O MAP

| Address         | Read/write | Register name | Register description                     |
|-----------------|------------|---------------|--|
| 00 <sub>H</sub> | (R/W)      | PDR0          | Port 0 data register                     |
| 01 <sub>H</sub> | (W)        | DDR0          | Port 0 data direction register           |
| 02 <sub>H</sub> | (R/W)      | PDR1          | Port 1 data register                     |
| 03 <sub>H</sub> | (W)        | DDR1          | Port 1 data direction register           |
| 04 <sub>H</sub> | (R/W)      | PDR2          | Port 2 data register                     |
| 05 <sub>H</sub> |            |               | Vacancy                                  |
| 06 <sub>H</sub> |            |               | Vacancy                                  |
| 07 <sub>H</sub> | (R/W)      | SYCC          | System clock control register            |
| 08 <sub>H</sub> | (R/W)      | STBC          | Standby control register                 |
| 09 <sub>H</sub> | (R/W)      | WDTC          | Watchdog timer control register          |
| 0A <sub>H</sub> | (R/W)      | TBCR          | Time-base timer control register         |
| 0B <sub>H</sub> | (R/W)      | WPCR          | Watch prescaler control register         |
| 0C <sub>H</sub> | (R/W)      | PDR3          | Port 3 data register                     |
| 0D <sub>H</sub> | (W)        | DDR3          | Port 3 data direction register           |
| 0E <sub>H</sub> | (R/W)      | PDR4          | Port 4 data register                     |
| 0F <sub>H</sub> | (W)        | DDR4          | Port 4 data direction register           |
| 10 <sub>H</sub> | (R/W)      | PDR5          | Port 5 data register                     |
| 11 <sub>H</sub> | (R)        | PDR6          | Port 6 data register                     |
| 12 <sub>H</sub> |            |               | Vacancy                                  |
| 13 <sub>H</sub> |            |               | Vacancy                                  |
| 14 <sub>H</sub> |            |               | Vacancy                                  |
| 15 <sub>H</sub> |            |               | Vacancy                                  |
| 16 <sub>H</sub> |            |               | Vacancy                                  |
| 17 <sub>H</sub> | (R/W)      | PIVE          | Port inverting operation enable register |
| 18 <sub>H</sub> | (R/W)      | TMCR          | 16-bit timer count register              |
| 19 <sub>H</sub> | (R/W)      | TCHR          | 16-bit timer count register (H)          |
| 1A <sub>H</sub> | (R/W)      | TCLR          | 16-bit timer count register (L)          |
| 1B <sub>H</sub> |            |               | Vacancy                                  |
| 1C <sub>H</sub> | (R/W)      | SMR           | Serial I/O mode register                 |
| 1D <sub>H</sub> | (R/W)      | SDR           | Serial I/O data register                 |
| 1E <sub>H</sub> |            |               | Vacancy                                  |
| 1F <sub>H</sub> |            |               | Vacancy                                  |

(Continued)

# MB89810A Series

(Continued)

| Address                            | Read/write    | Register name | Register description                         |
|------------------------------------|---------------|---------------|--|
| 20 <sub>H</sub>                    | (R/W)         | SMC1          | UART serial I/O mode control register 1      |
| 21 <sub>H</sub>                    | (R/W)         | SRC           | UART serial I/O rate control register        |
| 22 <sub>H</sub>                    | (R/W)         | SSD           | UART serial I/O status/data control register |
| 23 <sub>H</sub>                    | (R/W)         | SIDR/SODR     | UART serial I/O data control register        |
| 24 <sub>H</sub>                    | (R/W)         | SMC2          | UART serial I/O mode control register 2      |
| 25 <sub>H</sub>                    |               |               | Vacancy                                      |
| 26 <sub>H</sub>                    |               |               | Vacancy                                      |
| 27 <sub>H</sub>                    |               |               | Vacancy                                      |
| 28 <sub>H</sub>                    | (R/W)         | CNTR1         | PWM timer control register 1                 |
| 29 <sub>H</sub>                    | (R/W)         | CNTR2         | PWM timer control register 2                 |
| 2A <sub>H</sub>                    | (R/W)         | CNTR3         | PWM timer control register 3                 |
| 2B <sub>H</sub>                    | (W)           | COMR2         | PWM timer compare register 2                 |
| 2C <sub>H</sub>                    | (W)           | COMR1         | PWM timer compare register 1                 |
| 2D <sub>H</sub>                    |               |               | Vacancy                                      |
| 2E <sub>H</sub>                    |               |               | Vacancy                                      |
| 2F <sub>H</sub>                    | (R/W)         | PWCR          | Pulse width detection control register       |
| 30 <sub>H</sub>                    | (R/W)         | EIC1          | External interrupt 1 control register 1      |
| 31 <sub>H</sub>                    | (R/W)         | EIC2          | External interrupt 1 control register 2      |
| 32 <sub>H</sub>                    | (R/W)         | EI2E          | External interrupt 2 enable register         |
| 33 <sub>H</sub>                    | (R/W)         | EI2F          | External interrupt 2 flag register           |
| 34 <sub>H</sub>                    |               |               | Vacancy                                      |
| 35 <sub>H</sub> to 7A <sub>H</sub> |               |               | Vacancy                                      |
| 7B <sub>H</sub>                    |               |               | Vacancy                                      |
| 7C <sub>H</sub>                    | (W)           | ILR1          | Interrupt level register 1                   |
| 7D <sub>H</sub>                    | (W)           | ILR2          | Interrupt level register 2                   |
| 7E <sub>H</sub>                    | (W)           | ILR3          | Interrupt level register 3                   |
| 7F <sub>H</sub>                    | Not available | ITR           | Interrupt test register                      |

Note: Do not use vacancies.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

(V<sub>SS</sub> = 0.0 V)

| Parameter                              | Symbol             | Value                 |                       | Unit | Remarks   |
|--|--------------------|-----------------------|-----------------------|------|---|
|  |                    | Min.                  | Max.                  |      |   |
| Power supply voltage                   | V <sub>CC</sub>    | V <sub>SS</sub> - 0.3 | V <sub>SS</sub> + 7.0 | V    |   |
| Input voltage                          | V <sub>I1</sub>    | V <sub>SS</sub> - 0.3 | V <sub>CC</sub> + 0.3 | V    | Except P50 to P54                               |
|  | V <sub>I2</sub>    | V <sub>SS</sub> - 0.3 | V <sub>SS</sub> + 7.0 | V    | P50 to P54                                      |
| Output voltage                         | V <sub>O1</sub>    | V <sub>SS</sub> - 0.3 | V <sub>CC</sub> + 0.3 | V    | Except P50 to P54                               |
|  | V <sub>O2</sub>    | V <sub>SS</sub> - 0.3 | V <sub>SS</sub> + 7.0 | V    | P50 to P54                                      |
| "L" level maximum output current       | I <sub>OL</sub>    | —                     | 20                    | mA   | Peak value                                      |
| "L" level average output current       | I <sub>OLAV1</sub> | —                     | 4                     | mA   | Average value except pins other than P50 to P54 |
|  | I <sub>OLAV2</sub> | —                     | 10                    | mA   | Average value for P50 to P54                    |
| "L" level total maximum output current | ∑I <sub>OL</sub>   | —                     | 100                   | mA   | Peak value                                      |
| "L" level total average output current | ∑I <sub>OLAV</sub> | —                     | 40                    | mA   | Average value                                   |
| "H" level maximum output current       | I <sub>OH</sub>    | —                     | -20                   | mA   | Peak value                                      |
| "H" level average output current       | I <sub>OHAV</sub>  | —                     | -4                    | mA   | Average value                                   |
| "H" level total maximum output current | ∑I <sub>OH</sub>   | —                     | -50                   | mA   | Peak value                                      |
| "H" level total average output current | ∑I <sub>OHAV</sub> | —                     | -20                   | mA   | Average value                                   |
| Power consumption                      | P <sub>D</sub>     | —                     | 300                   | mW   |   |
| Operating temperature                  | T <sub>A</sub>     | -40                   | +85                   | °C   |   |
| Storage temperature                    | T <sub>stg</sub>   | -55                   | +150                  | °C   |   |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

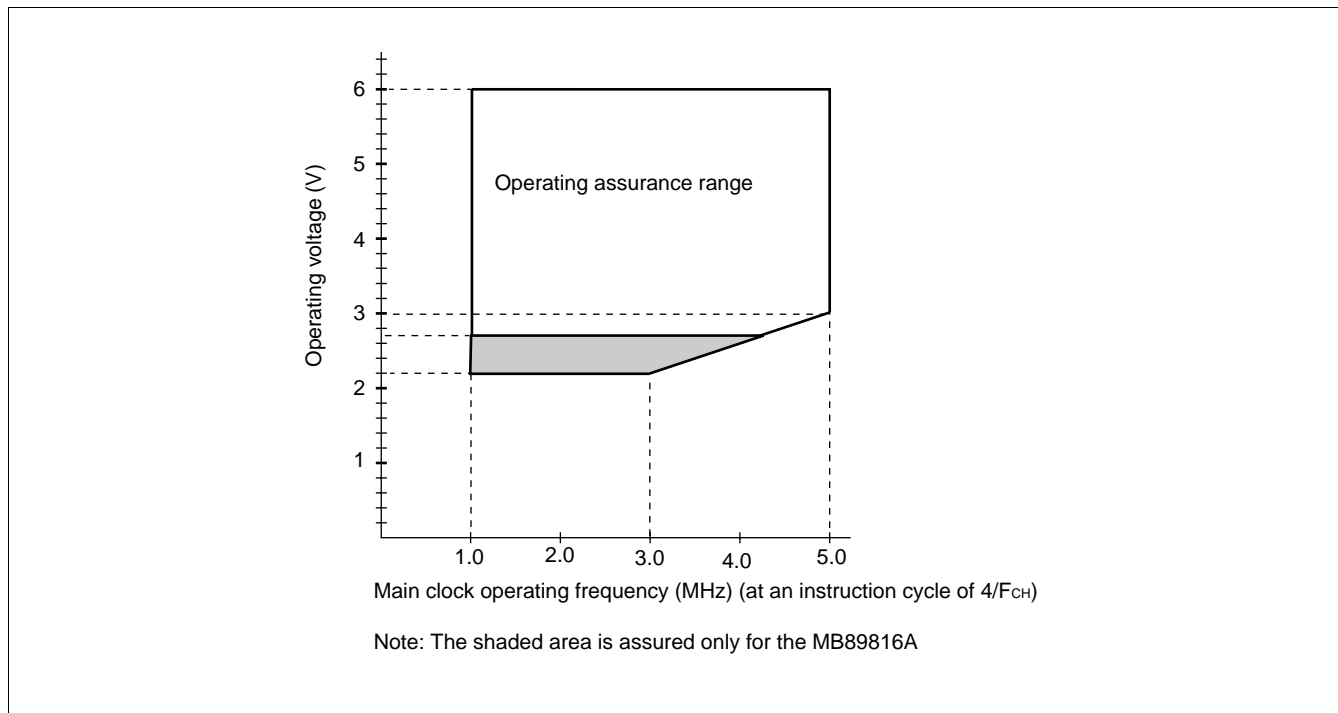
# MB89810A Series

## 2. Recommended Operating Conditions

( $V_{SS} = 0.0\text{ V}$ )

| Parameter                                 | Symbol   | Value          |                | Unit | Remarks                                    |
|---|----------|----------------|----------------|------|--|
|   |          | Min.           | Max.           |      |  |
| Power supply voltage                      | $V_{CC}$ | 2.2*           | 6.0            | V    | Normal operation assurance range MB89816A  |
|   |          | 2.7*           | 6.0            | V    | Normal operation assurance range MB89P817A |
|   |          | 1.5            | 6.0            | V    | Retains the RAM state in stop mode         |
| Open-drain output pin application voltage | $V_D$    | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V    | P50 to P54 (without pull-up resistor)      |
| Operating temperature                     | $T_A$    | -40            | +85            | °C   |  |

\*: These values vary with the operating frequency. See Figure 1.



**Figure 1 Operating Voltage vs. Main Clock Operating Frequency (for MB89816A)**

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB89810A Series

## 3. DC Characteristics

( $V_{CC} = +5.0\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter   | Symbol     | Pin  | Condition                                       | Value          |      |                | Unit          | Remarks                  |
|---|------------|--|---|----------------|------|----------------|---------------|--------------------------|
|   |            |  |   | Min.           | Typ. | Max.           |               |                          |
| “H” level input voltage                             | $V_{IH}$   | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54 (with pull-up resistor)             | —   | $0.7 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             |                          |
|   | $V_{IHS}$  | $\overline{RST}$ , MOD0, MOD1, P60 to P67, Peripheral input for port 3 and port 4              | —   | $0.8 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             |                          |
|   | $V_{IHS2}$ | P50 to P54 (without pull-up resistor)  | —   | $0.8 V_{CC}$   | —    | $V_{SS} + 6.0$ | V             |                          |
| “L” level input voltage                             | $V_{IL}$   | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54                                     | —   | $V_{SS} - 0.3$ | —    | $0.3 V_{CC}$   | V             |                          |
|   | $V_{ILS}$  | $\overline{RST}$ , MOD0, MOD1, P60 to P67, Peripheral input for port 3 and port 4              | —   | $V_{SS} - 0.3$ | —    | $0.2 V_{CC}$   | V             |                          |
| “H” level output voltage                            | $V_{OH}$   | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47                                     | $I_{OH} = -2.0\text{ mA}$                       | 2.4            | —    | —              | V             |                          |
| “L” level output voltage                            | $V_{OL1}$  | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P60 to P67             | $I_{OL} = 1.8\text{ mA}$                        | —              | —    | 0.4            | V             |                          |
|   | $V_{OL2}$  | P50 to P54   | $I_{OL} = 6\text{ mA}$<br>$V_{CC} = 3\text{ V}$ | —              | —    | 0.5            | V             |                          |
|   | $V_{OL3}$  | $\overline{RST}$   | $I_{OL} = 4.0\text{ mA}$                        | —              | —    | 0.4            | V             |                          |
| Input leakage current (Hi-z output leakage current) | $I_{LI1}$  | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P60 to P67, MOD0, MOD1 | $0.45\text{ V} < V_I < V_{CC}$                  | —              | —    | $\pm 5$        | $\mu\text{A}$ | Without pull-up resistor |
| Pull-up resistance                                  | $R_{PULL}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P54, P60 to P67, $\overline{RST}$       | $V_I = 0.0\text{ V}$                            | 25             | 50   | 100            | k $\Omega$    | With pull-up resistor    |

(Continued)

# MB89810A Series

(Continued)

( $V_{CC} = +5.0\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter             | Symbol  | Pin  | Condition   | Value |      |   | Unit      | Remarks   |
|-----------------------|---|--|---|-------|------|---|-----------|---|
|                       |   |  |   | Min.  | Typ. | Max.  |           |   |
| Power supply current* | I <sub>CC1</sub>  | V <sub>CC</sub>                                | F <sub>CH</sub> = 5 MHz<br>V <sub>CC</sub> = 5.0 V<br>t <sub>inst</sub> = 0.8 μs  | —     | 4    | 6   | mA        | MB89816A  |
|                       |   |  | —   | 4.8   | 7.5  | mA  | MB89P817A |   |
|                       | I <sub>CC2</sub>  |  | F <sub>CH</sub> = 5 MHz<br>V <sub>CC</sub> = 3.0 V<br>t <sub>inst</sub> = 6.4 μs  | —     | 0.4  | 0.6   | mA        | MB89816A  |
|                       |   |  | —   | 1.0   | 1.5  | mA  | MB89P817A |   |
|                       | I <sub>CCS1</sub>                                       |  | F <sub>CH</sub> = 5 MHz<br>V <sub>CC</sub> = 5.0 V<br>t <sub>inst</sub> = 0.8 μs  | —     | 1.2  | 1.8   | mA        | Sleep mode  |
|                       | I <sub>CCS2</sub>                                       |  | F <sub>CH</sub> = 5 MHz<br>V <sub>CC</sub> = 3.0 V<br>t <sub>inst</sub> = 12.8 μs | —     | 0.3  | 0.5   | mA        |   |
|                       | I <sub>CCL</sub>  |  | F <sub>CL</sub> = 32.768 kHz<br>V <sub>CC</sub> = 3.0 V                           | —     | 50   | 100   | μA        | Subclock mode   |
|                       |   |  |   | —     | 500  | 700   | μA        | MB89P817A   |
|                       | I <sub>CCLS</sub>                                       |  | F <sub>CL</sub> = 32.768 kHz<br>V <sub>CC</sub> = 3.0 V                           | —     | 15   | 50  | μA        | Subclock sleep mode                                     |
|                       | I <sub>CCCT</sub>                                       |  | F <sub>CL</sub> = 32.768 kHz<br>V <sub>CC</sub> = 3.0 V                           | —     | —    | 15  | μA        | Watch mode<br>Main clock stop mode at dual-clock system |
| I <sub>CCCH</sub>     | F <sub>CL</sub> = 32.768 kHz<br>V <sub>CC</sub> = 3.0 V | —  | —   | 10    | μA   | Subclock stop mode<br>Main clock stop mode at single-clock system |           |   |
| Input capacitance     | C <sub>IN</sub>   | Other than V <sub>CC</sub> and V <sub>SS</sub> | f = 1 MHz   | —     | 10   | —   | pF        |   |

\*: The measurement conditions of power supply current are as follows: the external clock and  $T_A = +25\text{ }^\circ\text{C}$ .



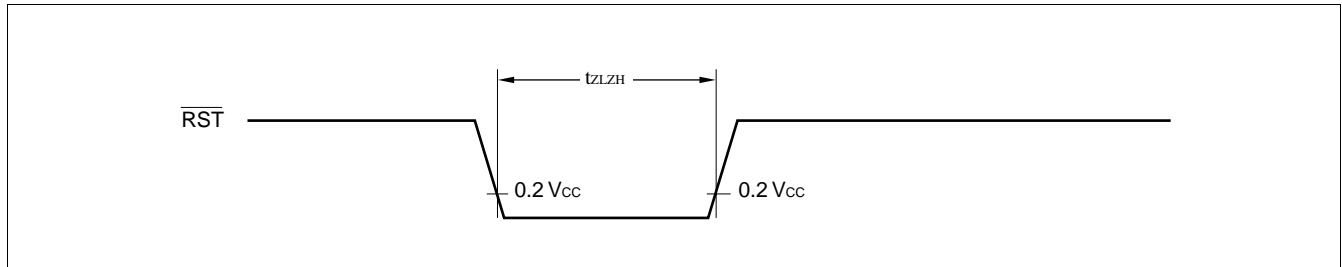
## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                               | Symbol           | Condition | Value              |      | Unit | Remarks |
|---|------------------|-----------|--------------------|------|------|---------|
|   |                  |           | Min.               | Max. |      |         |
| $\overline{\text{RST}}$ "L" pulse width | $t_{\text{LZH}}$ | —         | $48 t_{\text{CH}}$ | —    | ns   |         |

Note:  $t_{\text{CH}}$  is the cycle time of the main clock.



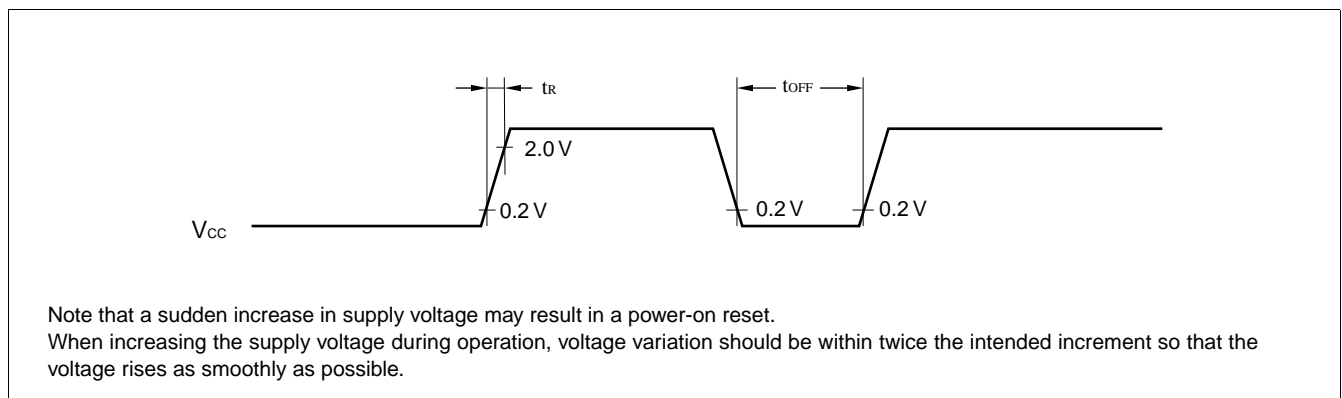
### (2) Power-on Reset

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter                 | Symbol           | Condition | Value |      | Unit | Remarks                      |
|---------------------------|------------------|-----------|-------|------|------|------------------------------|
|                           |                  |           | Min.  | Max. |      |                              |
| Power supply rising time  | $t_{\text{R}}$   | —         | —     | 50   | ms   | Power-on reset function only |
| Power supply cut-off time | $t_{\text{OFF}}$ |           | 1     | —    |      |                              |

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



Note that a sudden increase in supply voltage may result in a power-on reset.

When increasing the supply voltage during operation, voltage variation should be within twice the intended increment so that the voltage rises as smoothly as possible.

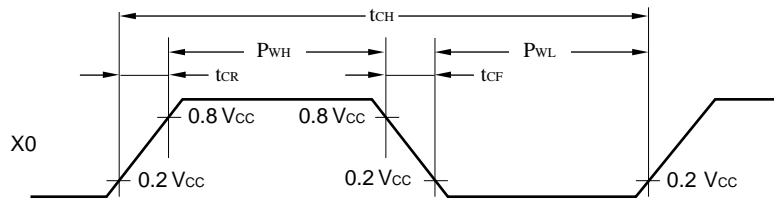
# MB89810A Series

## (3) Clock Timing

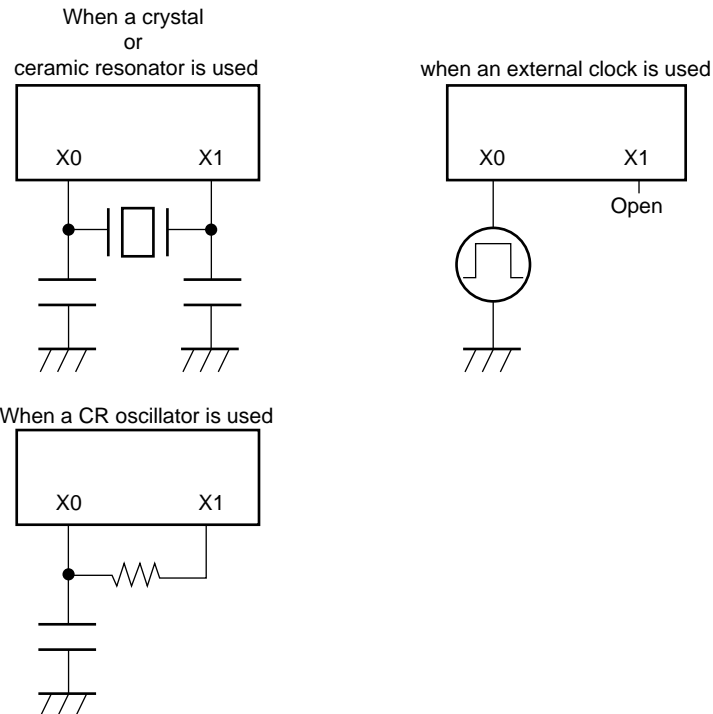
( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

| Parameter                           | Symbol                 | Pin      | Condition | Value |        |      | Unit          | Remarks        |
|-------------------------------------|------------------------|----------|-----------|-------|--------|------|---------------|----------------|
|                                     |                        |          |           | Min.  | Typ.   | Max. |               |                |
| Clock frequency                     | $F_{CH}$               | X0, X1   | —         | 1     | —      | 5    | MHz           |                |
|                                     | $F_{CL}$               | X0A, X1A |           | —     | 32.768 | —    | kHz           |                |
| Clock cycle time                    | $t_{CH}$               | X0, X1   |           | 200   | —      | 1000 | ns            |                |
|                                     | $t_{CL}$               | X0A, X1A |           | —     | 30.5   | —    | $\mu\text{s}$ |                |
| Input clock pulse width             | $P_{WH}$<br>$P_{WL}$   | X0       |           | 20    | —      | —    | ns            | External clock |
|                                     | $P_{WHL}$<br>$P_{WLL}$ | X0A      |           | —     | 15.2   | —    | $\mu\text{s}$ |                |
| Input clock rising/<br>falling time | $t_{CR}$<br>$t_{CF}$   | X0       |           | —     | —      | 10   | ns            | External clock |

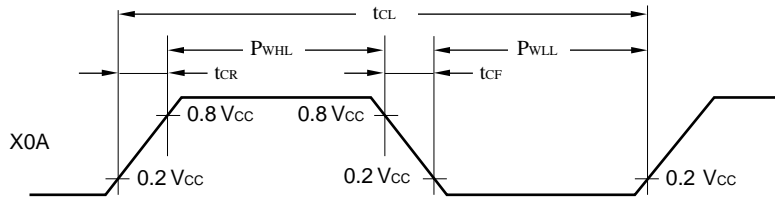
### X0 and X1 Timing and Conditions



### Main Clock Conditions

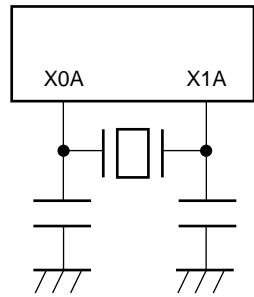


## X0A and X1A Timings and Conditions

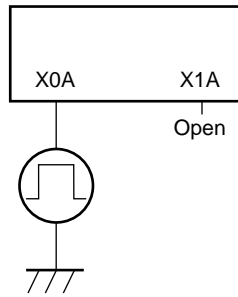


## Subclock Conditions

When a crystal or ceramic resonator is used



when an external clock is used



## (4) Instruction Cycle

| Parameter                                     | Symbol     | Value (typ)                    | Unit    | Remarks  |
|---|------------|--------------------------------|---------|--|
| Instruction cycle<br>(Minimum execution time) | $t_{inst}$ | $4/F_C, 8/F_C, 16/F_C, 64/F_C$ | $\mu s$ | $t_{inst} = 0.8 \mu s$ when operating at $F_C = 5 \text{ MHz}$ ( $4/F_C$ ) |
|   |            | $2/F_{CL}$                     | $\mu s$ | $t_{inst} = 61.036 \mu s$ when operating at $F_{CL} = 32.768 \text{ kHz}$  |

Note: When operating at 5 MHz, the cycle varies with the set execution time.

## (5) Serial I/O Timings

( $V_{CC} = +5.0 \text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$ )

| Parameter  | Symbol      | Pin                  | Condition                 | Value          |      | Unit | Remarks |
|--|-------------|----------------------|---------------------------|----------------|------|------|---------|
|  |             |                      |                           | Min.           | Max. |      |         |
| Serial clock cycle time                                  | $t_{SCYC1}$ | $\overline{SCK}$     | Internal shift clock mode | $2 t_{inst}$   | —    | ns   |         |
| $\overline{SCK} \downarrow \rightarrow SO$ time          | $t_{SLOV1}$ | $\overline{SCK}, SO$ |                           | -200           | 200  | ns   |         |
| Valid SI $\rightarrow \overline{SCK} \uparrow$           | $t_{VSH1}$  | SI, $\overline{SCK}$ |                           | $1/2 t_{inst}$ | —    | ns   |         |
| $\overline{SCK} \uparrow \rightarrow$ valid SI hold time | $t_{SHIX1}$ | $\overline{SCK}, SI$ |                           | $1/2 t_{inst}$ | —    | ns   |         |
| Serial clock "H" pulse width                             | $t_{SHSL}$  | $\overline{SCK}$     | External shift clock mode | $1 t_{inst}$   | —    | ns   |         |
| Serial clock "L" pulse width                             | $t_{LSLH}$  | $\overline{SCK}$     |                           | $1 t_{inst}$   | —    | ns   |         |
| $\overline{SCK} \downarrow \rightarrow SO$ time          | $t_{SLOV2}$ | $\overline{SCK}, SO$ |                           | 0              | 200  | ns   |         |
| Valid SI $\rightarrow \overline{SCK} \uparrow$           | $t_{VSH2}$  | SI, $\overline{SCK}$ |                           | $1/2 t_{inst}$ | —    | ns   |         |
| $\overline{SCK} \uparrow \rightarrow$ valid SI hold time | $t_{SHIX2}$ | $\overline{SCK}, SI$ |                           | $1/2 t_{inst}$ | —    | ns   |         |

Note: For information on  $t_{inst}$ , see "(4) Instruction Cycle".

# MB89810A Series

## (6) UART Timings

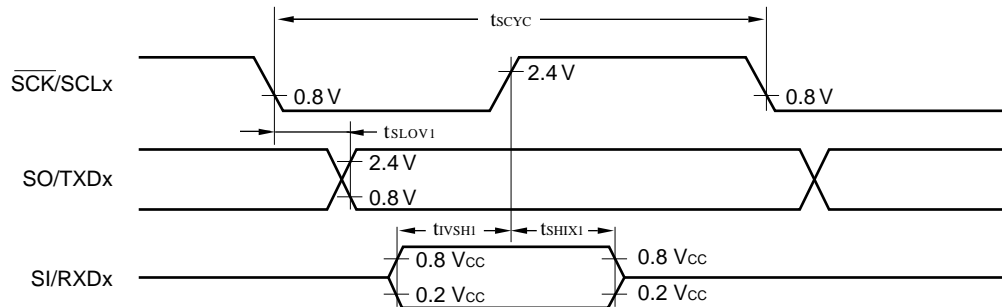
( $V_{CC} = +5.0 V \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter  | Symbol      | Pin           | Condition                    | Value          |      | Unit | Remarks |
|--|-------------|---------------|------------------------------|----------------|------|------|---------|
|  |             |               |                              | Min.           | Max. |      |         |
| Serial clock cycle time                          | $t_{SCYC}$  | SCL1,<br>SCL2 | Internal shift<br>clock mode | $2 t_{inst}$   | —    | ns   |         |
| SCL $\downarrow \rightarrow$ TXDx time           | $t_{SLOV1}$ | SCLx,<br>TXDx |                              | -200           | 200  | ns   |         |
| Valid RXDx $\rightarrow$ SCLx $\uparrow$         | $t_{IVSH1}$ | RXDx,<br>SCLx |                              | $1/2 t_{inst}$ | —    | ns   |         |
| SCLx $\uparrow \rightarrow$ valid RXDx hold time | $t_{SHIX1}$ | SCL1,<br>RXD2 |                              | $1/2 t_{inst}$ | —    | ns   |         |
| Serial clock "H" pulse width                     | $t_{SHSL}$  | SCL1,<br>SCL2 | External shift<br>clock mode | $1 t_{inst}$   | —    | ns   |         |
| Serial clock "L" pulse width                     | $t_{SLSH}$  |               |                              | $1 t_{inst}$   | —    | ns   |         |
| SCLx $\downarrow \rightarrow$ TXDx time          | $t_{SLOV2}$ | SCLx,<br>TXDx |                              | 0              | 200  | ns   |         |
| Valid RXDx $\rightarrow$ SCLx $\uparrow$         | $t_{IVSH2}$ | RXDx,<br>SCLx |                              | $1/2 t_{inst}$ | —    | ns   |         |
| SCLx $\uparrow \rightarrow$ valid RXDx hold time | $t_{SHIX2}$ | SCL1,<br>RXD2 |                              | $1/2 t_{inst}$ | —    | ns   |         |

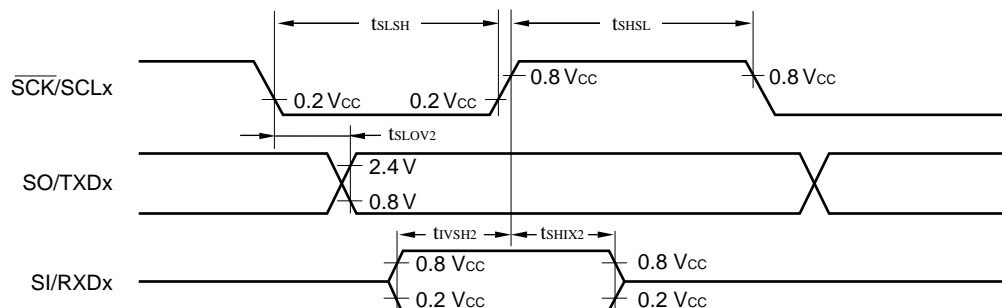
Notes: • For information on  $t_{inst}$ , see "(4) Instruction Cycle".

- The edge polarity for the SCLx input is assumed when LSEL bit = 0 for SMC2. The polarity is inverted when LSEL = 1.

### Internal Shift Clock Mode



### External Shift Clock Mode

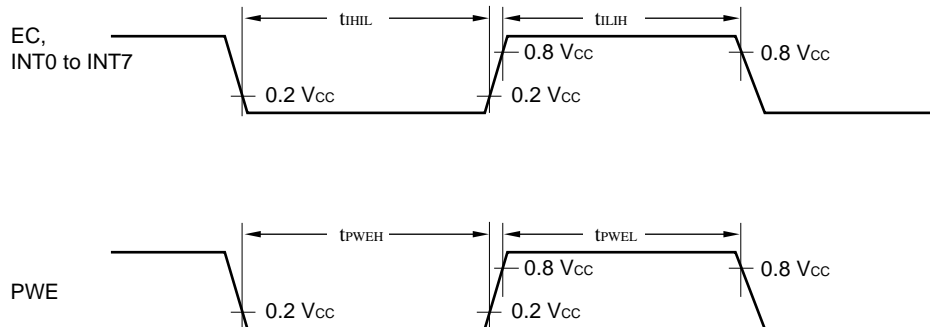


## (7) Peripheral Input Timings

( $V_{CC} = +5.0 V \pm 10\%$ ,  $A_{V_{SS}} = V_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

| Parameter  | Symbol     | Pin              | Condition | Value                                       |      | Unit | Remarks |
|--|------------|------------------|-----------|---|------|------|---------|
|  |            |                  |           | Min.  | Max. |      |         |
| Peripheral input "H" pulse width                             | $t_{ILIH}$ | EC, INT0 to INT7 | —         | $2 t_{inst}$                                | —    | ns   |         |
| Peripheral input "L" pulse width                             | $t_{IHIL}$ | EC, INT0 to INT7 | —         | $2 t_{inst}$                                | —    | ns   |         |
| "H" input pulse width of pulse width detection enable signal | $t_{PWEH}$ | PWE              | —         | $512 t_{CL} + 200$<br>or $480 t_{CL} + 200$ | —    | ns   |         |
| "L" input pulse width of pulse width detection enable signal | $t_{PWEL}$ |                  | —         | $512 t_{CL} + 200$<br>or $480 t_{CL} + 200$ | —    | ns   |         |

- Notes:
- For information on  $t_{inst}$ , see "(4) Instruction Cycle".
  - $t_{CL}$  represents the subclock cycle time.
  - The PWE pulse width value varies with the first divider selection bit of the watch prescaler. The pulse width is " $512 t_{CL} + 200$ " when divide by 16 is selected; or " $480 t_{CL} + 200$ " when divide by 15 is selected.



# MB89810A Series

## ■ MASK OPTIONS

| No. | Part number  | MB89816A                      | MB89P817A  |
|-----|--|-------------------------------|--|
|     | Specifying procedure   | Specify when ordering masking | Set with EPROM programmer  |
| 1   | Pull-up resistors <ul style="list-style-type: none"> <li>•P00 to P07, P10 to P17,</li> <li>•P30 to P37, P40 to P47,</li> <li>•P50 to P54, P60 to P67</li> </ul>  | Specify by pin                | Can be set per pin.<br>(P50 to P54 are available only for without a pull-up resistor.) |
| 2   | Power-on reset selection <ul style="list-style-type: none"> <li>•With power-on reset</li> <li>•Without power-on reset</li> </ul>   | Selectable                    | Setting possible   |
| 3   | Main clock oscillation (5 MHz) stabilization time selection* <ul style="list-style-type: none"> <li>•approx. <math>218/F_{CH}</math> (approx. 52.4 ms)</li> <li>•approx. <math>217/F_{CH}</math> (approx. 26.2 ms)</li> <li>•approx. <math>214/F_{CH}</math> (approx. 3.2 ms)</li> <li>•approx. <math>24/F_{CH}</math> (approx. 0 ms)</li> </ul> | Selectable                    | Setting possible   |
| 4   | Reset pin output selection <ul style="list-style-type: none"> <li>•With reset output</li> <li>•Without reset output</li> </ul>   | Selectable                    | Setting possible   |
| 5   | Selection either single- or dual-clock system <ul style="list-style-type: none"> <li>•Single clock</li> <li>•Dual clock</li> </ul>   | Selectable                    | Setting possible   |
| 6   | Main clock oscillator type selection <ul style="list-style-type: none"> <li>•Crystal or ceramic oscillator</li> <li>•CR</li> </ul>   | Selectable                    | Setting possible   |

$F_{CH}$ : Main clock frequency

\*: The main clock oscillation setting time is generated by dividing the main clock frequency. Note that the oscillation cycle is not stable immediately after oscillation is started. The settling time value in this data sheet should be used as a reference.

## ■ ORDERING INFORMATION

| Part number               | Package                             | Remarks |
|---------------------------|-------------------------------------|---------|
| MB89816APF<br>MB89P817APF | 64-pin Plastic QFP<br>(FPT-64P-M06) |         |



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